i.MX6Q/D USB

**Overview**

The USB module in the i.MX6x consists of 4 independent USB controllers. The OTG controller can be configured to work either as host controller or device controller. The H1, H2 and H3 controllers are Host only .



The Host controllers, including the host function in the OTG controller, provide full USB 2.0 host functionality including support for hubs.

The OTG device controller supports up to 8 bidirectional endpoints. Endpoint 0 is the default control endpoint and is always bidirectional (per USB 2.0 specification).  
IN and OUT directions of endpoints 1 through 7 are fully independent. Each can independently be configured as Control, Bulk, Interrupt or ISO.

**Transceivers**

USB transceivers convert the digital signals from the USB controller to signal levels and timing required on the USB bus.

The OTG and H1 controllers are intended for off-board USB connections. Each has an on-chip UTMI-plus compliant transceiver. The OTG controller uses USBPHY1, the H1 controller uses USBPHY2.   
Controllers H2 and H3 are intended for on-board connections and have a High Speed Inter-Chip interface (HSIC). This interface is a USB standard that allows for connecting to on-board devices without the need for a transceiver. The HSIC interface can also be used for off-board connections in combination with a HSIC hub.

**Clocks**

The USB controllers operate on 3 independent clocks.

Most of the controller’s logic runs on the ARM platform clock. This clock is controlled in the CCM module by register CCM\_CCGR6, bits CG0 (usb\_clk\_enable). This clock must be enabled before the USB module can be accessed.

The PHY clock clocks the logic that handles the USB bus timing, protocol and UTMI PHY interface. This clock is derived from the 480 MHz clock in the PHY. This clock will stop when the PHY is placed in low-power suspend mode unless it is forced to remain on.

The 32 KHz clock is always on in the system and clocks the power control logic of the USB controller. This logic monitors the USB lines when the PHY is in low-power mode and generates a wake-up interrupt when a wakeup event is detected.

**PLLs**

The USB module has 2 PLL modules associated that provide the low-jitter 480 MHz clock for the PHYs.

USBPLL1 generates the clock for the OTG controller, USBPLL2 for the Host1 controller.  
Host2 and Host3 use the clock from USBPLL1 for the HSIC interface and derived PHY clock.

**External signals**

T.B.D.

**API functions**

usb\_init\_clocks()

This function enables the USB clocks and PLLs.

usb \_phy\_init()

usb \_host\_init();

usb\_device\_init();

Configures and initializes the OTG controller for device operation, creates and initializes device queue heads and initi

**Host mode api**

usb\_qh\_init(